WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Tuesday, June 15, 2004

Hide?	Set Name	Query	Hit Count
		DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L12	L11 and (375/$3.ccls.)	40
☐	L11	takatori.in.	2598
☐	L10	L8 and l6	31
☐	L9	L8 and l5	397
☐	L8	=20000114	18657205
☐	L7	l4 and (dfe or (decision adj feedback adj equaliz$3)) and ((pre adj cursor$) or precursor$) and ((post adj cursor$) or postcursor$)	7
☐	L6	L5 and ((pre adj cursor$) or precursor$) and ((post adj cursor$) or postcursor$)	35
☐	L5	((timing$ or clock$3) near4 (recover$3 or detect$3)) and l3	436
☐	L4	(375/371.ccls. or 375/373.ccls. or 375/354.ccls. or 375/376.ccls. or 327/141.ccls. or 327/154.ccls. or 327/155.ccls. or 327/156.ccls. or 327/162.ccls.)	8377
☐	L3	(375/229.ccls. or 375/232.ccls. or 375/233.ccls. or 708/300.ccls. or 708/322.ccls. or 708/323.ccls)	2343
☐	L2	((timing$ or clock$3) near4 (recover$3 or detect$3)) and (dfe or (decision adj feedback adj equaliz$3)) near5 (FFE or (feed adj forward adj equaliz$3)) and ((pre adj cursor$) or precursor$) and ((post adj cursor$) or postcursor$)	18
☐	L1	((timing$ or clock$3) near4 (recover$3 or detect$3)) same (dfe or (decision adj feedback adj equaliz$3)) near5 (FFE or (feed adj forward adj equaliz$3)) same ((pre adj cursor$) or precursor$) same ((post adj cursor$) or postcursor$)	1

END OF SEARCH HISTORY

h e b b cg b chh e e f ff e ch e b c e

First Hit Fwd Refs

Generate Collection

L1: Entry 1 of 1 File: USPT Jul 2, 2002

DOCUMENT-IDENTIFIER: US 6414990 B1
TITLE: Timing recovery for a high speed digital data communication system based on adaptive equalizer impulse response characteristics

Detailed Description Text (33):
The above assumptions and observations form the basis for the following preferred timing recovery technique. Generally, a timing recovery element 700 may be suitably configured to measure the pre-cursor and post-cursor impulse responses of the FFE/DFE equalizer structure with, e.g., a pre-cursor energy measurement element 702 and a post-cursor energy measurement element 704 (see FIG. 7). The respective measurement elements 702, 704 may be configured to generate normalized measurement values such that an intelligent basis for comparison can be obtained. A comparator 706 performs a comparison analysis of the normalized pre-cursor and post-cursor response measurements to obtain a difference. It should be appreciated that measurement elements 702, 704 may be alternately configured to generate any desirable quantity based on the respective responses and that comparator 706 may be configured to process any suitable quantity associated with the pre-cursor and post-cursor responses.

h e b b g ee e f e e

First Hit Fwd Refs

Generate Collection

L1: Entry 1 of 1 File: USPT Jul 2, 2002

DOCUMENT-IDENTIFIER: US 6414990 B1
TITLE: Timing recovery for a high speed digital data communication system based on adaptive equalizer impulse response characteristics

Detailed Description Text (33):
The above assumptions and observations form the basis for the following preferred timing recovery technique. Generally, a timing recovery element 700 may be suitably configured to measure the pre-cursor and post-cursor impulse responses of the FFE/DFE equalizer structure with, e.g., a pre-cursor energy measurement element 702 and a post-cursor energy measurement element 704 (see FIG. 7). The respective measurement elements 702, 704 may be configured to generate normalized measurement values such that an intelligent basis for comparison can be obtained. A comparator 706 performs a comparison analysis of the normalized pre-cursor and post-cursor response measurements to obtain a difference. It should be appreciated that measurement elements 702, 704 may be alternately configured to generate any desirable quantity based on the respective responses and that comparator 706 may be configured to process any suitable quantity associated with the pre-cursor and post-cursor responses.

First Hit Fwd Refs

Generate Collection

L2: Entry 15 of 18 File: USPT Aug 11, 1998

DOCUMENT-IDENTIFIER: US 5793759 A
TITLE: Apparatus and method for digital data transmission over video cable using orthogonal cyclic codes

Drawing Description Text (11):
FIG. 9 represents the preferred process for resychronizing all RUs after the CU has changed its delay vector called the precursor process.

Detailed Description Text (100):
FIG. 9 represents the preferred process for resychronizing all RUs after the CU has changed its delay vector. This process will be called the precursor embodiment herein. This process starts with block 246 wherein the CU concludes that it must alter its delay vector to allow the farthest RUs to synchronize to the same frame as the nearest RUs. The CU, after reaching the conclusion that a change in its delay vector must be made, broadcasts a message to all RUs indicating when and by how much it will alter its delay vector.

Detailed Description Text (131):
The chip clock signal on line 348 of FIG. 12 is generated by a time base generator PLL 350 and is synchronized with the TDMA data stream by the action of the PLL in keeping both the chip clock and bit clock signals synchronized with the crystal oscillator reference signal. A block diagram of the time base generator 350 is shown in FIG. 18. A voltage controlled oscillator 353 operating at a frequency of 114.688 Mhz sets the basic operating frequency. The output frequency of the VCO on line 357 is divided by two by a divide-by-two counter 359. The result is coupled to one input of a multiplexer 361. The multiplexer has as its other input the crystal controlled oscillator frequency on line 363. The multiplexer switching is controlled by a bypass signal on line 365 so as to normally select the output of the counter 359 and couple it to output line 367. The PLL time base generator generates the bit clock signal on line 377 by dividing the frequency of the signal on line 367 by a factor of 7 in a divide-by-seven counter 369 to generate a bit clock signal on line 377 having a frequency of 8.192 Mhz. The chip clock signal on line 348 is generated by dividing the frequency on line 367 by a factor of 16 in a divide-by-16 counter 371 to generate a chip clock signal having a frequency of 3.548 Mhz. The bit clock and chip clock signals are kept synchronized to the crystal frequency by a phase detector 373 which compares the phase of the crystal signal to the phase of the bit clock signal and outputs a signal which is coupled to the frequency control input 375 of the VCO through a low pass filter 397. The bit clock signal and phase detector causes the PLL to force the transitions of the chip clock signal to line up properly with the bit clock transitions in the relationship of 16 periods of bit clock for every 7 periods of chip clock.

Detailed Description Text (183):
FIG. 26 is a more detailed diagram of the structure of the demodulator 460. The received analog signal from the shared transmission media is coupled on line 461 to the analog input of an A/D converter 463. The stream of digital data resulting from the analog-to-digital conversion is simultaneously fed to two multipliers 465 and 467. Multiplier 465 receives as its other input, a stream of digital values that define a sine wave having the same frequency as the RF carrier sine wave on line 437 in FIG. 24. Multiplier 467 receives as its other input, a stream of digital

values that define a cosine wave having the same frequency as the RF carrier cosine wave on line 427 in FIG. 24. The results output on lines 469 and 471 is a digital data stream which basically defines the mix products comprised of a fundamental carrier frequency and upper and lower sidebands. Digital filters 473 and 475 filter out the desired sidebands that contain the real and imaginary parts of each chip or result point that was transmitted. The stream of quadrature or imaginary components of the received chips are output on bus 477. The stream of inphase or real components of the received chips are output on bus 479. The receiver of FIG. 19 also includes conventional phase lock loop circuitry for clock recovery and carrier recovery. In other words, the receiver recovers the bit clock timing used by the CU and synchronizes to it using conventional phase lock loop circuitry and also recovers and synchronizes to the sine and cosine carriers used by the CU to transmit the symbol data. These clock and carrier signals are then used for transmissions by the RU to the CU so that the CU can coherently communicate with the RU's without having to synchronize to different clock and carrier signals used by the RU's. In alternative embodiments, the RUs can use their own clock and carrier signals which are unrelated to the CU's versions and the CU can contain its own phase lock loop circuitry to recover these signals and synchronize to them in order to demodulate and interpret the data transmitted by the RUs.

Detailed Description Text (185):
After the linear arrays of real and imaginary components for a symbol are stored in memory 464, the result for each symbol is an array of received chip points in a received chip space having a real axis and an imaginary axis. The mapping by orthogonal code transformation from the constellation of possible input points shown in FIG. 21 leads to a constellation of possible points in a received chip space. A detector 466 examines the points in each of the arrays and compares the received chip points they define against the legitimate possible points in the received chip space. The detector, othewise known as a slicer, is a known type of circuit and no further details are necessary herein. The function of the detector is to restore the gain and phase of the received signal, recover the chip clock therefrom and lock onto it so as to be in synchronization with the transmitter, determine the boundaries of each chip and determine the values for the I and Q coordinates of each received chip and compare the I and Q coordinates of each received chip point against the closest points in the constellation of legitimate possible points in the received chip space that could have been transmitted. The detector also locks the frequency of its local oscillators in the detector generating the sine and cosine signals used for demodulation to the phase and frequency of the sine and cosine carriers encoded in the data. The detector then makes a preliminary decision as to which of the possible legitimate points in the received chip constellation each received chip is likely to be.

Detailed Description Text (235):
Referring to FIG. 32, there is shown a flow chart for a ranging process carried out by the RUs using a binary tree algorithm. The process starts with one or more RUs that are not in frame synchronization but which wish to achieve frame synchronization so as to be able to send data to the CU. These RUs first must synchronize their receivers to broadcasts on the control channel from the CU so that they can receive status commands from the CU which control their activities during the ranging process. The RUs can synchronize to the CU broadcasts themselves without assistance from or the need to send anything to the CU by recovering the system clock signal from the periodic broadcasts of the barker code signals every frame from the CU. Once this has happened, test 668 determines that control channel signals can be received and ranging can start. Until this happens, path 670 is taken to wait state 672 and block 674 to idle until the RU receiver synchronizes to the CU and can receive its broadcasts.

Detailed Description Text (246):
In an alternative embodiment, the output of of the matched filter 762 is filtered by a feed forward equalization (FFE) filter 764 which functions to cut down on

precursor intersymbol interference. The FFE filter is an adaptive FIR filter. Adaptive FIR filters and many of the other digital signal processing components of the circuitry disclosed herein are known and are discussed in detail in Elliott, Handbook of Digital Signal Processing: Engineering Applications, (Academic Press, Inc. San Diego, 1987), ISBN 0-12-237075-9, which is hereby incorporated by reference. In the preferred embodiment, the FFE filter 764 is placed between circuits 765 and 767 to filter the data on bus 769.

Detailed Description Text (249):
The despread data on bus 776 is simultaneously read by a crosstalk detector 778 which functions to determine the amount of interference between adjacent codes and also plays a role in clock recovery so that all RU and CU receivers and transmitters can be synchronized to the same clock. Crosstalk between channels encoded with adjacent cyclic, orthogonal codes always comes from adjacent channels and happens when the data encoded with adjacent cyclic CDMA codes do not arrive precisely aligned in time. In other words, to have zero crosstalk, the clock time at which the first chip of a symbol transmitted on one channel spread with a cyclic CDMA code arrives at the receiver must be exactly the same time as the clock time at which the first chip of a symbol transmitted on an adjacent channel spread with an adjacent cyclic code. A slippage of one chip clock means complete overlap and total crosstalk since adjacent cyclic codes are generated by shifting the code by one place to the right. A slippage or misalignment of less than one complete chip clock will mean that some crosstalk exists. The crosstalk detector detects the amount of crosstalk affecting each chip of each channel by subtracting the amplitude of a corresponding chip of the next sequential channel from the amplitude of the corresponding chip the next previous channel.

Detailed Description Text (250):
The amount of crosstalk or clock tracking error detected by the crosstalk detector 778 is fed on line 780 as an error signal to a control loop logic 781 which outputs a clock phase/frequency correction voltage on line 782. This signal is coupled to the phase/frequency control input of a voltage controlled crystal oscillator 784 which generates a clock reference signal on line 786.

Detailed Description Text (256):
The feed forward equalizer 764 functions to eliminate or substantially reduce precursor intersymbol interference, and a decision feedback equalizer 820 functions to reduce or eliminate post cursor intersymbol interference. If a transmitter were to send an impulse signal on one symbol with adjacent symbols empty, the receivers in an ideal system would receive the impulse with zeroes on either side of it. However, because of system impairments, the receivers will receive an impulse and there will be some nonzero data in symbols on either side of the impulse. The nonzero data in symbols that precede the impulse symbol in time are precursor intersymbol interference. The FFE circuit 764 removes this interference. The nonzero data in symbols that follow the impulse symbol in time is postcursor interference which is removed by the DFE circuit 820. Both the DFE and FFE circuits are FIR filters with adaptive coefficients which they receive on buses 842 and 844, respectively, from a least mean square calculation circuit 830. The FIR filters are given initial values for the adaptive coefficients that are close enough to allow the adaptation process to proceed. These preset coefficients are supplied via buses 824 and 822.

Detailed Description Text (257):
The adaptaption process for the FIR filters is carried out by a least mean squared calculation circuit 830. This circuit receives a signal on bus 831 from a difference calculation circuit 832. The difference calculation circuit calculates the error between the desired data on bus 836 and available data on bus 834 and outputs this error on bus 831. The least mean square (LMS) calculation circuit then correlates this error with the input data on bus 769 to the FFE and DFE FIR filters read via bus 838 (this assumes the FFE FIR filter is located at its preferred

position just before subtractor 767 so as to receive data from bus 769 and output data to the + input of the subtractor 767). If the FFE FIR filter is located where shown in FIG. 34, bus 838 connects to bus 840 instead of bus 769. After the LMS calculation circuit makes this correlation, it send adaptation coefficients to the FIR filters via buses 842 and 844. The LMS circuit implements a calculation which is based upon the fact that the needed change in the adaptive coefficients to the adaptive FIR filters 764 and 820 is proportional to the error on bus 831 times the conjugate of the data being input to the filters. In other words, the error is multiplied by complex numbers representing the received chips which have had the signs of their Q or imaginary components inverted.

Detailed Description Text (258):
The DFE filter eliminates or reduces post cursor interference by supplying a subtraction value on bus 846 to subtractor 767. The data sent by the DFE filter on bus 846 is subtracted from the data on bus 769 (or from the output of the FFE filter, depending upon its position). Eliminating the precursor interference and post cursor interference from the data on the bus 834 allows the slicer 800 and a Viterbi Decoder 850 to make better decisions about what chips were actually sent despite the channel impairments. The LMS, DFE and FFE circuits can be eliminated in some simple embodiments with, for example, only 4 points in their constellations. But to get more data throughput, more complex constellations are needed, and in such a situation, the points are closer together and ISI interference makes decisional discrimination between the constellation points more difficult. This creates a need for the above described ISI elimination circuitry.

Detailed Description Text (265):
Clock Recovery

Detailed Description Text (266):
The RUs cannot begin the process of ranging until they have synchronized to the master clock of the system. The master clock runs in the CU and is encoded into the downstream data sent from the CU to the RUs during the gaps. The downstream data is comprised of the barker codes sent every frame by the CU to the RUs during the gaps between frames. All the RUs synchronize to this downstream data by extracting the master clock signal therefrom thereby achieving clock synchronization and frame synchronization. Frame synchronization, as that term is used in the clock recovery context, only means the RUs know when the CUs frames start. Frame synchronization, as the term is used for ranging or training purposes, refers to the establishment of the proper transmit frame timing reference delays in each RU such that each RU hits the middle of the gap with its ranging pulses such that all symbols transmitted by each RU, regardless of differences in location and propagation delay arrive simultaneously at the CU for despreading. Clock recovery from the barker codes transmitted during the gaps is done using phase lock loop 880, voltage controlled oscillator 784, phase detector 778, control loop 781 and loop filter in frame detector 882 in FIG. 34. The phase detector 778 determines the phase error by comparing the phase of the clock signal derived from the barker code received from the CU to the phase of the local oscillator clock generated by the PLL 880 and generates a phase error signal on bus 780. This phase error signal is passed by control loop 781 to the voltage controlled oscillator 784 which changes its frequency in a direction to eliminate the phase error. The phase of the local oscillator clock is derived from a signal on bus 884 from time base generator 886. The time base generator generates the needed bit clock, byte clock, chip clock and other timing signals from the local oscillator signal received on line 888.

First Hit Fwd Refs

Generate Collection

L2: Entry 17 of 18 File: USPT Dec 3, 1996

DOCUMENT-IDENTIFIER: US 5581585 A
** See image for Certificate of Correction **
TITLE: Phase-locked loop timing recovery circuit

Abstract Text (1):
A timing recovery apparatus for recovering the timing from sparse timing information in multi-level or partial response codes. The timing recovery apparatus includes a switch for sampling an incoming line code signal according to a selectable sample rate, a feed forward equalizer for filtering the sampled signal, a decision feedback equalizer for cancelling intersymbol interference in the filtered signal and for recovering the timing in the sampled signal. The timing recovery circuit creates a phase correction signal in response to a signal received from the feed forward equalizer and thereby control the sample rate of the sample switch so that the signal-to-noise ratio at the node before the decision is maximized. The voltage controlled crystal oscillator may be controlled within a certain frequency range by using a second phase detector which compares the phase of the signal controlling the sampling of the incoming line code with a reference clock.

Brief Summary Text (3):
This invention relates to a timing recovery circuit, and more particularly, to a phase lock loop circuit for recovering the timing from sparse timing information in multi-level or partial response codes.

Brief Summary Text (5):
Digital data transmission has become increasingly important and accordingly, the need to provide more reliable digital data transmission continues to propel the search for superior systems for recovering timing from a received line code. In order to utilize the bandwidth of the channel effectively, many digital transmission systems have begun to use band efficient multi-level line codes, such as 2B1Q (two-bit coded into one quat symbol) and partial response codes. Although multi-level line codes improve system performance, these line codes make the timing recovery and the pulse shaping more difficult because of the non-self timed characteristics of the line code itself.

Brief Summary Text (6):
The prior art traditionally used analog signal processing of the incoming data signal to derive a timing signal. However, most digital receivers use digital processing techniques to recover the digital information which is modulated on the incoming pulse train. Consequently, the received signal is sampled at discrete time intervals and converted to digital amplitude magnitudes. Any additional processing is accomplished using digital circuitry. To minimize cost and complexity, the incoming signal is usually sampled at the lowest possible rate, i.e., the baud rate. However, sampling at the baud rate creates aliasing distortion when the analog signal waveform is reconstructed. Therefore, analog timing recovery techniques cannot generally be used in digital receivers which operate at the baud rate.

Brief Summary Text (7):
One prior art technique for overcoming this problem is taught by Kurt H. Mueller

and Markus Muller in an article entitled "Timing Recovery in Digital Synchronous Data Receivers," IEEE TRANSACTIONS ON COMMUNICATIONS, Volume COM-20, May 1976, pages 516-530, herein incorporated by reference. In this article, a preselected timing function is used to describe the optimal sampling instant. The coefficient values of this timing function are then estimated from the arriving signal samples. However, since timing jitter depends on the actual pulse sequence transmitted as well as the impulse response, the timing function estimates have a relatively high variance. Further, if the channel response is heavily distorted by the bridged taps, this technique cannot be used.

Brief Summary Text (8):
U.S. Pat. No. 5,020,078 to Crespo issued May 28, 1991, herein incorporated by reference, provides a technique for recovering the transmitted signal from the received signal by using a decision feedback equalizer to estimate and then remove the intersymbol interference. A second decision feedback equalizer is used to estimate the timing of the sampling pulse. An optimum timing phase is derived by driving the sampling clock with a phase adjustment signal optimizing the amplitude of the sampling pulse. However, the decision feedback equalizer may be subjected to precursor intersymbol interference which cannot be cancelled.

Brief Summary Text (9):
There is a need, therefore, for a simple device for recovering timing from multi-level codes transmitted over heavily distorted channels.

Brief Summary Text (11):
To overcome the limitations in the prior art described above, and to overcome other limitations that will become apparent upon reading and understanding the present specification, the present invention discloses a timing recovery device which includes means for sampling an incoming line code signal according to a selectable sample rate, feed forward equalizing means for filtering the sampled signal, and a decision feedback equalizer unit for cancelling intersymbol interference in the filtered signal and for recovering the timing in the sampled signal.

Brief Summary Text (12):
The timing recovery circuit creates a phase correction signal in response to a signal received from the feed forward equalizer and thereby controls the sample rate of the sample means.

Brief Summary Text (13):
The timing recovery circuit is basically for the base band digital transmission but it is also effective for the modulated system as well once the signal is demodulated. The timing recovery circuit also extracts timing information from the baud rate signal, so the signal processing in a transceiver can be simplified.

Brief Summary Text (14):
The present invention solves the above-described problems by providing a phase locked loop timing recovery circuit which adjusts the rate that the original line code signal is sampled so that the signal-to-noise ratio at the node before the decision feedback equalizer is maximized.

Brief Summary Text (19):
Another aspect of the present invention is that the voltage controlled crystal oscillator is controlled within a certain frequency range by using a second phase detector which compares a reference clock with the phase of the control signal for the first sampling device.

Drawing Description Text (3):
FIG. 1 is a general block diagram of the timing recovery circuit in accordance with the invention;

Drawing Description Text (4):
FIG. 2 is a detailed block diagram of the timing recovery circuit in accordance with the invention;

Drawing Description Text (8):
FIG. 6 is a detailed block diagram of the timing recovery circuit having an automatic threshold calculator in accordance with a second embodiment of the invention;

Drawing Description Text (9):
FIG. 7 is a detailed block diagram of the timing recovery circuit having the coefficient for the (N-1)th tap automatically calculated in accordance with a third embodiment of the invention; and

Drawing Description Text (10):
FIG. 8 is a detailed block diagram of the timing recovery circuit having improved phase accuracy in accordance with a fourth embodiment of the invention.

Detailed Description Text (3):
The present invention provides a phase lock loop circuit for recovering the timing from sparse timing information in multi-level or partial response codes.

Detailed Description Text (4):
FIG. 1 show a general illustrative digital data system 10 in which applicants' inventive timing recovery technique is embodied. Information is transmitted over a telecommunications network. Such data may include high-speed data sent over the telecommunications network in a full-duplex manner at a predetermined pulse or baud-rate. In order to utilize the band width of the channel effectively, many digital transmission systems use band efficient multi-level line codes, such as 2B1Q (two-bit coded into one quat symbol) and partial response codes. In a sampled-data system, the accurate reconstruction of such high-speed, sparse timing signals sent over relatively long lengths of a twisted-pair channel is a formidable task. Noise and linear distortion introduced over the transmission media caused received signals to be significantly different from those that are transmitted.

Detailed Description Text (6):
By way of example, such data samples are assumed herein to be received over line 12 of FIG. 1. The foregoing clearly illustrates the advantage and importance of being able to reliably recover clock or timing signals.

Detailed Description Text (7):
The input signal received over line 12 is sampled according to a clock signal by switch 14. The signal 16 controlling the sample rate is divided down by the divider 18 to the appropriate speed such as the symbol rate. After being adjusted by automatic gain control (AGC) 20, the signal is fed to the feed forward equalizer (FFE) 22. The feed forward equalizer 22 adapts to the line response so that the node immediately prior to the decision feedback equalizer unit (DFE) 24 sees no precursor intersymbol interference (ISI) which cannot be cancelled by the DFE.

Detailed Description Text (9):
Now referring to FIG. 2, the feed forward equalizer 22 is a N-tap transversal filter, which is conceptually a delay line 100 tapped at predefined intervals. Each tap 110 is connected through a variable gain 120 to a summing bus 130. The final tap 140 has a fixed value of unity (i.e., the coefficient value of Nth tap equals 1), and is not adaptive. The sampling speed at the input is assumed to be the symbol rate. In other words, one value of the input signal is sampled per symbol period and is fed to the feed forward equalizer 22. Each tap 110 sends an adjusted signal to the summing node wherein the post-cursor intersymbol interference is cancelled by the decision feedback equalizer unit 24.

Detailed Description Text (11):
As illustrated in FIG. 2, the decision feedback equalizer unit 24 consists of an adder 170 having an output to a decision block or threshold detector 180. The decision block 180 generates the recovered timing signal 190. In turn, the output 190 of the decision block 180 is fed back into a decision feedback equalizer circuit 200 which estimates the post cursor intersymbol interference. Thus, the decision feedback equalizer 200 provides feedback to cancel any intersymbol interference in the signal received from the feed forward equalizer.

Detailed Description Text (14):
In accordance with the LMS algorithm, the initialization of the timing recovery circuit will be described. At the beginning of the link activation, the feed forward equalizer coefficients 120, except for Nth tap 140 which is unity, are set to zero. These coefficients start converging based on the least mean square algorithm. For example:

Detailed Description Text (18):
As the convergence of feed forward equalizer 22 and decision feedback equalizer unit 24 proceed, the feed forward equalizer coefficients 120 adapt to the channel and noise characteristic and converge to values where the addition of the intersymbol interference and the additive noise at the decision node is minimized. However, since the Nth feed forward equalizer tap 140 is fixed to unity value and the other coefficient values 120 are limited to the value C.sub.max, the feed forward equalizer 22, according to the present invention, maintains a group delay constant, i.e., N symbol periods. Thus, the feed forward equalizer coefficient values 120 are a function of the phase difference between the sampling clock 16 and the transmitted phase of the incoming signal 12.

Detailed Description Text (26):
During the link activation period before the feed forward equalizer 22 and decision feedback equalizer unit 24 become adaptive, the second phase detector 600 is connected to the loop filter 28. After controlling VCXO frequency offset from 200 ppm to 60 ppm, the phase-locked loop uses the threshold basis phase detector 600 and the total phase-locked loop to track the incoming phase. As mentioned above, the second phase detector 600 is referenced to an accurate external clock (.+-.30 to 40 ppm) source 610.

CLAIMS:

1. A timing recovery circuit, comprising: sampling means for sampling an incoming line code signal according to a selectable sample rate;

a feed forward equalizer, coupled to the sampling means, comprises a transversal filter for receiving and filtering the sampled incoming line code signal, the transversal filter comprising N taps, each of the N taps providing an output, N-1 multipliers for multiplying each of the outputs of N-1 of the N taps by a respective coefficient factor, each of the N-1 multipliers providing an output, and an adder for adding the respective outputs of the N-1 multipliers and the output of the Nth tap to produce a filtered signal that is adapted to the sampled incoming line code signal;

a decision feedback equalizer, coupled to the feed forward equalizer, for cancelling an intersymbol interference in the filtered signal, for adjusting the filtering in the feed forward equalizer, and for recovering timing information from the filtered signal;

phase determining means, coupled to a multiplier in the feed forward equalizer, the phase determining means receiving a coefficient factor from the multiplier and creating a phase correction signal in response thereto;

h e b b g eeef e e b c e

sample control means, coupled to the phase determining means and the sampling means, for creating a sample control signal for selecting the sample rate of the sampling means in response to the phase correction signal generated by the phase determining means.

2. The timing recovery apparatus of claim 1, wherein the decision feedback equalizer further comprises decision feedback means for estimating intersymbol interference, accumulating means for receiving the filtered signal of the feed forward equalizer and the estimated intersymbol interference from the decision feedback means, and decision means for receiving the output of the accumulating means and for generating the recovered timing information.

3. The timing recovery apparatus of claim 1, wherein the phase determining means further comprises a comparator for comparing a threshold level to the coefficient factor received from the feed forward equalizer and a loop filter, coupled to the output of the comparator, for generating the phase correction signal in response thereto.

4. The timing recovery apparatus of claim 3, wherein the threshold level is a predetermined constant threshold level.

5. The timing recovery apparatus of claim 3, wherein the threshold level is generated by the decision feedback equalizer.

6. The timing recovery apparatus of claim 1, wherein the sample control means is a voltage controlled crystal oscillator.

7. A timing recovery circuit, comprising:

sampling means for sampling an incoming line code signal according to a selectable sample rate;

a transversal filter means, coupled to the sampling means, for filtering the sampled signal, said transversal filter means having N delay taps, each of the taps providing an output, the transversal filter means further comprising N-1 coefficient means, each coupled to one of N-1 of the N taps, for multiplying the respective output of the N-1 taps by a respective coefficient factor, and an adder for adding the outputs of the N-1 coefficient means to the output of the Nth tap;

decision feedback equalizer means, coupled to the transversal filter means, for estimating intersymbol interference in the output of the transversal filter means and for generating an error signal fed back to the transversal filter means;

accumulating means for receiving the output of the transversal filter means and the estimated intersymbol interference from the decision feedback equalizer means, for accumulating the estimated symbol interference and the output of the transversal filter means, and for generating an output in response thereto;

decision means, coupled to the accumulating means, for receiving the output of the accumulating means and for recovering timing information from the sampled signal;

phase determining means, coupled to the transversal filter means, for comparing a coefficient value for the (N-1)th tap to a threshold level and for generating a phase correction signal in response thereto; and

sample control means, coupled to the phase determining means and the sampling means, for creating a sample control signal for selecting the sample rate of the sample means in response to the phase correction signal.

8. The timing recovery apparatus of claim 7, wherein the threshold level is a

predetermined constant threshold level.

9. The timing recovery apparatus of claim 7, wherein the threshold level is generated in response to the error signal from the error decision feedback equalizer means.

10. The timing recovery apparatus of claim 7, wherein the sample control means is a voltage controlled crystal oscillator.

11. A timing recovery circuit, comprising:

first sampling means for sampling an incoming line code signal according to a first sample rate;

a feed forward equalizer, coupled to the first sampling means, the feed forward equalizer further comprising a transversal filter means for receiving and filtering the sampled incoming line code signal, the transversal filter means having N taps, each of the N taps providing an output, N-1 coefficient means for multiplying the outputs of N-1 of the N taps by a respective coefficient factor, and an adder for adding the outputs of the N-1 coefficient means and the output of the Nth tap to produce a filtered signal that is adapted to the sampled incoming line code signal;

a decision feedback equalizer, coupled to the feed forward equalizer, for cancelling intersymbol interference in the filtered signal, for recovering timing information from the sampled signal, and for generating an error signal in response thereto for adjusting the filtered signal in the feed forward equalizer;

phase determining means, coupled to the decision feedback equalizer, for creating a phase correction signal in response to the recovered timing information and the error signal; and

sample control means, coupled to the phase determining means and the first sampling means, for creating a sample control signal for selecting a new sample rate for the sample means in response to the phase correction signal generated by the phase determining means.

12. The timing recovery apparatus of claim 11, further comprising means, coupled to the feed forward equalizer and the phase determining means, for automatically calculating a threshold level resulting in the highest signal-to-noise ratio at the input of the decision feedback equalizer.

13. The timing recovery apparatus of claim 11, wherein the feed forward equalizer further comprises a transversal filter means having N taps, each of the N taps providing an output, a first coefficient factor control means, coupled to N-2 of the N taps, for modifying a coefficient factor to the N-2 taps in response to the error signal, a second coefficient factor control means, coupled to the (N-1)th tap, for modifying a coefficient factor to the (N-1)th tap in response to the error signal, and an adder for adding the output of the Nth tap to the outputs of the first and second coefficient factor control means.

14. The timing recovery apparatus of claim 11, wherein the phase determining means further comprises a loop filter, automatic threshold calculation means, coupled to the error decision feedback equalizer, for generating a threshold level signal in response to the error signal, and comparator means, coupled to the loop filter and the threshold calculation means, for generating a signal in response to the threshold level signal and the coefficient factor value from the (N-1)th tap.

15. The timing recovery apparatus of claim 11 wherein the phase determining means further comprises:

a multiplier, coupled to the decision feedback equalizer, for generating a pulse train in response to the error signal and the recovered timing signals;

second sampling means, coupled to the multiplier for sampling the pulse train, the second sampling means sampling the incoming signal according to a second selectable sample rate;

a loop filter, coupled to the second sampling means, for providing a voltage output;

a second sample control means, coupled to the loop filter, for creating a sampling control signal for regulating the first sample rate of the first sampling means in response to the voltage output of the loop filter; and

phase comparison means, coupled to the output of the second sample control means and to a reference clock, for comparing the phase of the sampling control signal to the phase of the reference clock, the phase comparison means generating a sampling control signal for regulating the second sample rate of the second sampling means in response thereto.